EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	3591	341/126,144,150,152.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/06/26 08:52
L2	2731	341/144.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/06/26 08:53
L3	267	341/144.ccls.	US-PGPUB	AND	ON	2006/06/26 08:53
L4	25	(digital ADJ1 analog or dac or d ADJ1 a) (high ADJ1 (frequency or frequencies)) carrier (finite or fir)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2006/06/26 08:54
L5	0	(digital ADJ1 analog or dac or d ADJ1 a) (high ADJ1 (frequency or frequencies)) carrier (finite or fir) and l3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2006/06/26 08:54
L6	0	(digital ADJ1 analog or dac or d ADJ1 a) (high ADJ1 (frequency or frequencies)) carrier (finite or fir) and l2	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2006/06/26 08:54
L7	0	(digital ADJ1 analog or dac or d ADJ1 a) (high ADJ1 (frequency or frequencies)) carrier (finite or fir) and l1	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2006/06/26 08:55
L8	0	(digital ADJ1 analog or dac or d ADJ1 a) (frequency or frequencies) carrier (finite or fir) and l1	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2006/06/26 08:55

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L9	60	(digital ADJ1 analog or dac or d ADJ1 a) (frequency or frequencies) (finite or fir) and l1	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2006/06/26 08:56
L10	48	(digital ADJ1 analog or dac or d ADJ1 a) (frequency or frequencies) (finite or fir) and l2	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2006/06/26 08:56
L11	6	(digital ADJ1 analog or dac or d ADJ1 a) (frequency or frequencies) (finite or fir) and l3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2006/06/26 08:56
L12	25	(digital ADJ1 analog or dac or d ADJ1 a) (frequency or frequencies) (finite or fir) and l4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	SAME	ON	2006/06/26 08:56
L13	1	(digital ADJ1 analog or dac or d ADJ1 a) (frequency or frequencies) (finite or fir) and l4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/06/26 08:57
L14	15	(digital ADJ1 analog or dac or d ADJ1 a) (frequency or frequencies) (finite or fir) and l1	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/06/26 08:57
L15	10	(digital ADJ1 analog or dac or d ADJ1 a) (frequency or frequencies) (finite or fir) and l2	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/06/26 08:57
L16	1	(digital ADJ1 analog or dac or d ADJ1 a) (frequency or frequencies) (finite or fir) and l3	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2006/06/26 08:57

Terms used **dac fir frequency** Found **120** of **178,880**

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1 Analogue and mixed-signal design: Double-sampling single-loop sigma-delta modulator topologies for broadband applications

Mohammad Yavari, Omid Shoaei, Angel Rodriguez-Vazquez

March 2006 **Proceedings of the conference on Design, automation and test in Europe: Proceedings DATE '06**

Publisher: European Design and Automation Association

Full text available: pdf(250.76 KB) Additional Information: full citation, abstract, references

This paper presents novel double sampling high order single-loop sigma-delta modulator structures for wideband applications. To alleviate the quantization noise folding into the inband frequency region, two previously reported techniques are used. The DAC sampling paths are implemented with the single capacitor approach and an additional zero is placed at the half of the sampling frequency of the modulator's noise transfer function (NTF). The detrimental effect of this additional zero on both th ...

2 RF circuit design and design methodology: A 10Gb/s transmitter with multi-tap FIR pre-emphasis in 0.18μm CMOS technology

Miao Li, Tad Kwasniewski, Shoujun Wang, Yuming Tao

January 2005 **Proceedings of the 2005 conference on Asia South Pacific design automation ASP-DAC '05**

Publisher: ACM Press

Full text available: pdf(772.00 KB) Additional Information: full citation, abstract, references

A 10Gb/s current mode logic (CML) transmitter with multi-tap finite impulse response (FIR) pre-emphasis has been implemented in 0.18μm CMOS technology. A half-rate clock retiming circuit for generating symbol-spaced data is proposed to alleviate the speed requirement of the traditional full-rate clock retiming. HSPICE simulation results of a 5-tap FIR transmitter show that the closed eye over a 34" FR4 backplane can be opened to 0.72UI at 10Gb/s. The power dissipation of the transmitter is 50 ...

3 Poster session 1: A new power-area efficient 4-PAM full-clock CMOS pre-emphasis transmitter for 10Gb/s serial links

Fei Yuan

April 2006 **Proceedings of the 16th ACM Great Lakes symposium on VLSI GLSVLSI '06**

Publisher: ACM Press

Full text available: pdf(242.32 KB) Additional Information: full citation, abstract, references, index terms

A new area-power efficient 4-PAM full-clock pre-emphasis CMOS transmitter for 10-Gb/s

serial links is proposed. The transmitter reduces the chip area and power consumption by minimizing the number of DACs for 4-PAM pre-emphasis and the DC power consumption of each DAC. The number of DACs is set by the number of pre-emphasis taps and is independent of the number of parallel bits. The power consumption of each DAC is lowered by modulating the DC current in accordance with the level of output curre ...

Keywords: Gbps serial link transmitters

4 A high-speed FIR digital filter with CSD coefficients implemented on FPGA

Mitsuru Yamada, Akinori Nishihara

January 2001 **Proceedings of the 2001 conference on Asia South Pacific design automation**

Publisher: ACM Press

Full text available: pdf(100.64 KB) Additional Information: full citation, abstract, references, index terms

A very fast and low-complexity FIR digital filter on FPGA is presented. Multipliers in the filter whose coefficients are expressed as canonic signed digit (CSD) code are realized with wired-shifters, adders and subtracters. The critical path is minimized by insertion of pipeline registers and is equal to the propagation delay of an adder. The number of pipeline registers is limited by using an equivalent transformation on a signal flow graph. The price paid for the 100% speedup is 5% increa ...

5 Poster session IV: A high performance QAM receiver for digital cable TV with integrated A/D and FEC decoder

Bo Shen, Junhua Tian, Zheng Li, Jianing Su, Qianling Zhang

January 2005 **Proceedings of the 2005 conference on Asia South Pacific design automation ASP-DAC '05**

Publisher: ACM Press

Full text available: pdf(391.37 KB) Additional Information: full citation, abstract, references

A DVB-C/ITU J.83-A compliant QAM (Quadrature Amplitude Modulation) demodulator suitable for digital cable TV is proposed, which can support 4~256QAM with variable bit rate up to 80Mbps. It integrates a 10-bit 40MSPS ADC, (204,188) Reed-Solomon decoder as well as a convolutional interleaver. The chip is implemented in SMIC 0.25um CMOS technology with die size of 3.5x3.5 mm^2. It features wide carrier offset acquisition range, robust demodulation algorithm and small circuit area.

6 Frequency-domain compatibility in digital filter BIST

Laurence Goodby, Alex Orailoğlu

June 1997 **Proceedings of the 34th annual conference on Design automation DAC '97**

Publisher: ACM Press

Full text available: pdf(255.07 KB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

We examine frequency-domain issues in the design and selectionof on-chip test generators for built-in self-test (BIST) of high-performancedigital filters. Test-generator/circuit compatibility isidentified as a significant factor in testing large filters. A fault-injectionexperiment is used to show that when an incompatible testgenerator is used, high fault coverage (over 99%) does not guaranteethat all serious faults will be detected. The frequency-domaincharacteristics of some basic test genera ...

7 Improved Design Methodology for High-Speed High-Accuracy Current Steering D/A Converters

Miquel Albiol, Jose Luis Gonzalez, Eduard Alarcon

March 2003 **Proceedings of the conference on Design, Automation and Test in Europe**

- Volume 1 DATE '03
Publisher: IEEE Computer Society
Full text available: pdf(1.19 MB) Additional Information: full citation, abstract, index terms
Publisher Site

This paper describes a sizing and design methodology for high-speed high-accuracy current steering D/A converters taking into account mismatching in all the transistors of the current source cell.The presented method allows a more accurate selection of the optimal design point without introducing arbitrary safety margins,as was done in the previous literature.This methodology has been applied to the design of a CMOS 12-bit 400 MHz current-steering segmented D/A converter.Commercial CAD tools are ...

8 Achieving 550 MHz in an ASIC methodology
D. G. Chinnery, B. Nikolic, K. Keutzer
June 2001 **Proceedings of the 38th conference on Design automation**
Publisher: ACM Press
Full text available: pdf(1.21 MB) Additional Information: full citation, abstract, references, citings, index terms

Typically, good automated ASIC designs may be two to five times slower than handcrafted custom designs. At last year's DAC this was examined and causes of the speed gap between custom circuits and ASICs were identified. In particular, faster custom speeds are achieved by a combination of factors: good architecture with well-balanced pipelines; compact logic design; timing overhead minimization; careful floorplanning, partitioning and placement; dynamic logic; post-layout transistor and wire ...

Keywords: ASIC, clock, comparison, custom, frequency, speed, throughput

9 A HW/SW co-design environment for multi-media equipments development using inverse problem
F. Suzuki, H. Koizumi, M. Hiramine, K. Yamamoto, H. Yasuura, K. Okino
March 1997 **Proceedings of the 5th International Workshop on Hardware/Software Co-Design**
Publisher: IEEE Computer Society
Full text available: pdf(728.10 KB) Additional Information: full citation, abstract
Publisher Site

Multimedia equipment development must provide functions that are adjusted to human sensibilities. Realization of such functions depends on how the three transfer levels of perception, recognition and susceptibility are handled. In this paper, we deal with perception by employing an inverse problem to characterize the system and correctly reproduce signals. To accommodate recognition and susceptibility, we propose an optimization method in which results are compared repeatedly with a model of hum ...

Keywords: audio circuitry, conceptual stage, cost estimates, development cycle reduction, evaluation, filter design, hardware/software codesign environment, human recognition characteristics, human sensibilities, inverse problem, multimedia communication, multimedia equipment development, netlist generation, numerical models, optimization method, perception, performance estimates, playback, repeated results comparison, semiconductor circuits, semiconductor production, signal reproduction, susceptibility, system response, television receiver

10 System-level power optimization: techniques and tools
Luca Benini, Giovanni de Micheli

April 2000 **ACM Transactions on Design Automation of Electronic Systems (TODAES),** Volume 5 Issue 2
Publisher: ACM Press

Full text available: pdf(385.22 KB) Additional Information: full citation, abstract, references, citings, index terms

This tutorial surveys design methods for energy-efficient system-level design. We consider electronic sytems consisting of a hardware platform and software layers. We consider the three major constituents of hardware that consume energy, namely computation, communication, and storage units, and we review methods of reducing their energy consumption. We also study models for analyzing the energy cost of software, and methods for energy-efficient software design and compilation. This survery ...

11 A methodology for efficient high-level dataflow simulation of mixed-signal front-ends of digital telecom transceivers

Gerd Vandersteen, Piet Wambacq, Yves Rolain, Petr Dobrovolný, Stéphane Donnay, Marc Engels, Ivo Bolsens
June 2000 **Proceedings of the 37th conference on Design automation**
Publisher: ACM Press

Full text available: pdf(241.33 KB) Additional Information: full citation, abstract, references, citings, index terms

The explosion of the telecommunications market requires miniaturization and cost-effective realization of the front-ends of transceivers for digital telecommunications. New architectures must therefore be simulated at high level. Current methodologies and corresponding tools suffer from common drawbacks, such as lower accuracy, slow simulation speed, etc. A new methodology has been developped for the efficient simulation, at the architectural level, of mixed-signal front-ends of digital tel ...

12 Technology mapping, buffering, and bus design: Synthesizing optimal filters for crosstalk-cancellation for high-speed buses

Jihong Ren, Mark Greenstreet
June 2003 **Proceedings of the 40th conference on Design automation**
Publisher: ACM Press

Full text available: pdf(228.84 KB) Additional Information: full citation, abstract, references, index terms

We present practical algorithms for the synthesis of crosstalk cancelling equalizing filters. We examine designs optimized for the traditional $l2$ metric and introduce an approach based on the $l\infty$ metric. We compare the two approaches for realistic buses with tight wire spacings. We show bandwidth improvements of up to a factor of 2 using crosstalk cancellation when compared with no filtering or independent pre-emphasis for each wire. Using $l\infty$ optimization, we achi ...

Keywords: buses, crosstalk, equalizing filters, optimal synthesis

13 Technologies and devices for low-power: Characterizing and modeling minimum energy operation for subthreshold circuits

Benton H. Calhoun, Anantha Chandrakasan
August 2004 **Proceedings of the 2004 international symposium on Low power electronics and design**
Publisher: ACM Press

Full text available: pdf(373.68 KB) Additional Information: full citation, abstract, references, index terms

Subthreshold operation is emerging as an energy-saving approach to many new applications. This paper examines energy minimization for circuits operating in the subthreshold region. We show the dependence of the optimum V DD for a given

technology on design characteristics and operating conditions. Solving equations for total energy provides an analytical solution for the optimum V DD and V T to minimize energy for a given frequency in subthreshold operation. SPICE simulations of a 200K transisto ...

Keywords: energy model, minimum energy point, subthreshold circuits, subthreshold model

14 Progress in logic and arithmetic circuit optimisation: Optimizing high speed arithmetic circuits using three-term extraction

Anup Hosangadi, Farzan Fallah, Ryan Kastner

March 2006 **Proceedings of the conference on Design, automation and test in Europe: Proceedings DATE '06**

Publisher: European Design and Automation Association

Full text available: pdf(303.88 KB) Additional Information: full citation, abstract, references

Carry Save Adder (CSA) trees are commonly used for high speed implementation of multi-operand additions. We present a method to reduce the number of the adders in CSA trees by extracting common three-term subexpressions. Our method can optimize multiple CSA trees involving any number of variables. This optimization has a significant impact on the total area of the synthesized circuits, as we show in our experiments. To the best of our knowledge, this is the only known method for eliminating comm ...

15 Low delay-power product CMOS design using one-hot residue coding

William A. Chren

April 1995 **Proceedings of the 1995 international symposium on Low power design**

Publisher: ACM Press

Full text available: pdf(102.70 KB) Additional Information: full citation, references, citings, index terms

16 Efficient analog test methodology based on adaptive algorithms

Luigi Carro, Marcelo Negreiros

May 1998 **Proceedings of the 35th annual conference on Design automation**

Publisher: ACM Press

Full text available: pdf(225.70 KB) Publisher Site Additional Information: full citation, abstract, references, index terms

This papers describes a new, fast and economical methodology totest linear analog circuits based on adaptive algorithms. To theauthors knowledge, this is the first time such technique is used totest analog circuits, allowing complete fault coverage. The paperpresents experimental results showing easy detection of soft,large-deviation and hard faults, with low cost instrumentation.Components variations from 5% to 1% have been detected, asthe comparison parameter (output error power) varied from30 ...

17 Synthesis of multiplier-less FIR filters with minimum number of additions

Mahesh Mehendale, S. D. Sherlekar, G. Venkatesh

December 1995 **Proceedings of the 1995 IEEE/ACM international conference on Computer-aided design**

Publisher: IEEE Computer Society

Full text available: pdf(476.50 KB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

Abstract: In this paper we present optimizing transformations to minimize the number of additions+subtractions in both the direct form (/spl Sigma/ A/sub i/X/sub n-i/ based) and its transposed form (Multiple Constant Multiplication based) implementation of FIR filters.

These transformations are based on the iterative elimination of 2-bit common subexpressions in the coefficients binary representations. We give detailed description of the algorithms and present results for eight low pass FIR filt ...

Keywords: FIR filters, MCM based structures, binary representations, circuit CAD, iterative elimination, low pass FIR filters, network synthesis, optimizing transformations

18 Microprocessor architecture: Frequent loop detection using efficient non-intrusive on-chip hardware

Ann Gordon-Ross, Frank Vahid

October 2003 **Proceedings of the 2003 international conference on Compilers, architecture and synthesis for embedded systems**

Publisher: ACM Press

Full text available: pdf(278.07 KB) Additional Information: full citation, abstract, references, index terms

Dynamic software optimization methods are becoming increasingly popular for improving software performance and power. The first step in dynamic optimization consists of detecting frequently executed code, or "critical regions." Previous critical region detectors have been targeted to desktop processors. We introduce a critical region detector targeted to embedded processors, with the unique features of being very size and power efficient, and being completely non-intrusive to the software's exec ...

Keywords: dynamic optimization, frequent loop detection, frequent value profiling, hardware profiling, hot spot detection, on-chip profiling, runtime profiling

19 New decompilation techniques for binary-level co-processor generation

G. Stiff, F. Vahid

May 2005 **Proceedings of the 2005 IEEE/ACM International conference on Computer-aided design ICCAD '05**

Publisher: IEEE Computer Society

Full text available: pdf(435.99 KB) Additional Information: full citation, abstract

Existing ASIPs (application-specific instruction-set processors) and compiler-based co-processor synthesis approaches meet the increasing performance requirements of embedded applications while consuming less power than high-performance gigahertz microprocessors. However, existing approaches place restrictions on software languages and compilers. Binary-level co-processor generation has previously been proposed as a complementary approach to reduce impact on tool restrictions, supporting all lan ...

20 The future of timing closure: Efficient timing closure without timing driven placement and routing

Miodrag Vujkovic, David Wadkins, Bill Swartz, Carl Sechen

June 2004 **Proceedings of the 41st annual conference on Design automation**

Publisher: ACM Press

Full text available: pdf(278.42 KB) Additional Information: full citation, abstract, references, index terms

We have developed a design flow from Verilog/VHDL to layout that mitigates the timing closure problem, while requiring no timing driven placement or routing tools. Timing issues are confined to the cell sizer, allowing the placement algorithm to focus solely on net lengths, resulting in superior layout densities and much lower power. The primary enablers to this new technology are: 1) gridded transistor sizing, 2) variable die routing that allows each net to be routed in the shortest possible le ...

Keywords: digital design flow, gate sizing, placement and routing, timing closure

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